

CLAIMS

What is claimed is:

- 5 1. A method of cell placement and clock tree synthesis comprising steps of:
- (a) identifying critical paths in an integrated circuit design;
- (b) partitioning the integrated circuit design into
- 10 a timing group for each of the critical paths;
- (c) assigning each flip-flop in a critical path to a timing group corresponding to the critical path;
- (d) performing a cell placement to minimize a
- 15 function of propagation delay and maximum distance between flip-flops within each timing group; and
- (e) constructing a clock sub-net for each timing group.
2. The method of Claim 1 wherein each timing
- 20 group contains only flip-flops that are included in a critical path.
3. The method of Claim 1 further comprising a
- step of replacing a flip-flop in a critical path with a
- 25 flip-flop in a non-critical path connected to the critical path.

4. The method of Claim 3 further comprising a step of inserting a clock skew between the critical path and the non-critical path.

5 5. The method of Claim 1 wherein flip-flops in connected critical paths are assigned to the same timing group.

6. The method of Claim 1 wherein every flip-flop that is included in a critical path is assigned to a timing group.

7. The method of Claim 1 further comprising a step of coupling a clock buffer to the clock sub-net so that the clock buffer is equidistant from each flip-flop in the timing group.

8. The method of Claim 7 further comprising a step of coupling a clock signal to the clock buffer from a clock tree.

9. The method of Claim 7 wherein the clock tree is a balanced clock tree.

10. A computer program product for cell placement and clock tree synthesis comprising:
a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

- (a) identifying critical paths in an integrated circuit design;
- 5 (b) partitioning the integrated circuit design into a timing group for each of the critical paths;
- (c) assigning each flip-flop in a critical path to a timing group corresponding to the critical path;
- 10 (d) performing a cell placement to minimize a function of propagation delay and maximum distance between flip-flops within each timing group; and
- (e) constructing a clock sub-net for each timing group.

15 11. The computer program product of Claim 10 wherein each timing group contains only flip-flops that are included in a critical path.

20 12. The computer program product of Claim 10 further comprising a step of replacing a flip-flop in a critical path with a flip-flop in a non-critical path connected to the critical path.

25 13. The computer program product of Claim 12 further comprising a step of inserting a clock skew between the critical path and the non-critical path.

14. The computer program product of Claim 10 wherein flip-flops in connected critical paths are assigned to the same timing group.

5 15. The computer program product of Claim 10 wherein every flip-flop that is included in a critical path is assigned to a timing group.

10 16. The computer program product of Claim 10 further comprising a step of coupling a clock buffer to the clock sub-net so that the clock buffer is equidistant from each flip-flop in the timing group.

15 17. The computer program product of Claim 16 further comprising a step of coupling a clock signal to the clock buffer from a clock tree.

20 18. The computer program product of Claim 17 wherein the clock tree is a balanced clock tree.